Paper No. 23

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

_____

Ex parte SOHEIL SHAMS
and DAVID B. SHU

_____

Appeal No. 1997-0917
Application 08/309,565

_____

ON BRIEF

_____

Before KRASS, JERRY SMITH and HECKER, ***Administrative Patent Judges***.

HECKER, ***Administrative Patent Judge***.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 13, all claims pending in the application.

The invention relates to computer architecture, and in particular, to a dynamically reconfigurable switch for connecting processing elements in processor arrays in Single

Instruction Stream Multiple Data Stream (SIMD) multi-processor architectures. As depicted in Figure 1, each processing element 10 is arranged on a two dimensional lattice 12 and is connected to its neighbors through dynamically reconfigurable switches 14. Switches 14, as shown in Figure 3, connect four of the processing elements in the array into a group in accordance with either a broadcast instruction of the controller or a special communication instruction held in one processing element of the group. A multiplexer unit is connected to each data line, the controller and to a configuration register. It is adapted to load the special communication instruction from the one processing element in the group into a configuration register and to operate in accord with either the broadcast instruction from the controller or the contents of the configuration register to select one of the four data lines as a source of data and applying the data therefrom to a source output port. Similarly, a demultiplexer unit is connected to each data line, the controller and to the configuration register, as well as to the source output port of the multiplexer unit. The demultiplexer is adapted to operate in accord with either

the broadcast instruction from the controller or the contents of the configuration register to select one of the four data lines and applying the data from the source output port of the multiplexer unit thereto. (Specification-pages 4 and 5.)

Representative independent claim 1 is reproduced as follows:

1. In a SIMD architecture having a two dimensional array of processing elements, where a controller broadcasts at least one broadcast instruction to all processing elements in the array, a dynamically reconfigurable switching means useful to connect four of the processing elements in the array into a group in accordance with either the broadcast instruction of the controller or a special communication instruction held in one selected processing element of the group, the switch comprising:

at least one dataline connected to each of the processing elements in the group;

a multiplexer means connected to each data line and to the controller and to a configuration register external to any processing element of the group, said configuration register controllable by any of the processing elements in the group, for loading the special communication instruction from the one selected processing element in the group into the configuration register and to operate in accord with either the broadcast instruction from the controller or the contents of the configuration register to select one of the data lines as a source of data and applying the data therefrom to a source output port; and

a demultiplexer means connected to each data line and to the controller and to said configuration register, and directly connected to a source output port of the multiplexer means, to operate in accord with either the broadcast

instruction from the controller or the contents of the configuration register to select one of the data lines and applying the data received directly from the source output port of the multiplexer means thereto.

The Examiner relies on the following reference:

Li 5,058,001 Oct. 15, 1991

Claims 1 through 13 stand rejected under 35 U.S.C. § 103 as being unpatentable over Li.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the brief and answer for the respective details thereof.

OPINION

After a careful review of the evidence before us, we will not sustain the rejection of claims 1 through 13 under 35 U.S.C. § 103.

The Examiner has failed to set forth a ***prima facie*** case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the reasonable teachings or suggestions found in the prior art, or by a reasonable inference to the artisan contained in such teachings or suggestions. ***In re Sernaker***,

702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." ***Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.***, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995) (***citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.***, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied***, 469 U.S. 851 (1984)).

With regard to the rejection of claims 1 through 13, Appellants argue that the Examiner is redefining the architecture of Li to identify alternate processing elements in Li as being reconfigurable switches for purposes of emulating the reconfigurable switches claimed. Appellants state:

> It is not valid for the Examiner to identify some processing elements in Li as "switches" and other processing elements in Li as "processing elements" simply to find some correspondence with the limitations of Appellant[s'] Claims 1, 2, and 3. (Brief-page 7.)

As pointed out by our reviewing court, we must first determine the scope of the claim. "[T]he name of the game is

the claim." ***In re Hiniker Co.***, 150 F.3d 1362, 1369, 47 USPQ2d 1523,1529 (Fed. Cir. 1998). Li discloses an array of processors, ***each having*** a hopping circuit which is a switch much like Appellants' switch. The fact that Li has a processor and a switch in each element does not detract from Li meeting Appellants' claim language. The mere designation of one of Li's elements as a switch since it contains a switch, or a processor since it contains a processor, is a choice of language that is consistent with the structure being designated. Likewise, we find the Examiner's designations not inconsistent with Appellants' claim language.

In the same vein Appellants urge "[T]he Examiner just ignores the remaining elements of the selected processing element, such as the ALU, sink register, and memory." (Brief-page 7.) However, we agree with the Examiner. Appellants use the claim term ***comprising*** which is inclusive and fails to exclude unrecited elements (answer-page 14).

Appellants argue that the structure of Li's switch differs from that recited in claim 1 in that Appellants' demultiplexer is claimed as ***directly connected*** to the source

output port of the multiplexer, while Li's demultiplexer and multiplexer are ***separated*** by a sink register.

The Examiner responds that the ***direct connection***

> is not a patentable distinction, but rather an engineering choice. ... The function of the sink register is to act as a closed-coupler between the MUX and DEMUX (see column 6, lines 11-16). This function can be incorporated into the control register file, since Li suggests that the content of register file can be loaded to or from the sink register (see column 5, lines 25-31). (Answer-page 16.)

We do not agree with the Examiner. The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch***, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), ***citing In re Gordon***, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." ***Para-Ordnance Mfg. v. SGS Importers Int'l***, 73 F.3d at 1087, 37 USPQ2d at 1239, ***citing W. L. Gore & Assocs.,***

Inc. v. Garlock, Inc., 721 F.2d at 1551, 1553, 220 USPQ at 311, 312-13.

Li contains two registers, one located in the processor section (file register 2) and one located in the hopping (switch) section (sink register 11). Li's sink register holds data before transferring it out through the DEMUX. Data may be placed into the sink register by either the MUX or the register file. Li's sink register performs a function not provided for by Appellants' ***direct connection***. Thus, removing this function from Li is not suggested or obvious over Li.

Since the ***direct connection*** limitation is recited in both independent claims 1 and 6, we will not sustain the 35 U.S.C. § 103 rejection of these claims.

The remaining claims on appeal also contain the above limitations discussed in regard to claims 1 and 6 and thereby, we will not sustain the rejection as to these claims.

We have not sustained the rejection of claims 1 through 13 under 35 U.S.C. § 103. Accordingly, the Examiner's decision is reversed.

REVERSED

Errol A. Krass Administrative Patent Judge	)	
Jerry Smith Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
Stuart N. Hecker Administrative Patent Judge	)	

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